

### **REMARKS**

Claims 1 - 16 are pending in the present application. By this Amendment, claims 1-3, 5-8, 10, 11 and 13-16 have been amended and claims 4 and 12 have been canceled. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated October 13, 2004.

#### **Allowable Subject Matter:**

Applicants gratefully acknowledge the indication in item 9 of the Action that claims 1-3, 5-11 and 13-16 are allowable albeit for the new claim objections to claims 1-3, 5-8, 10, 11 and 13-16 set forth in item 4, pages 2-5, of the Action, which are addressed below.

#### **Claim Objections:**

Claims 1-3, 5-8, 10, 11 and 13-16 are objected to in item 4, pages 2-5, of the Action due to various informalities.

With regard to the objection of claim 1, discussed in the bridging paragraph between pages 2 and 3 of the Action, the Examiner takes the position that the first and second product-sum calculating means do not clearly embody the invention, since “the first and remaining part of the received signal and the corresponding first and remaining part of the generated spreading sequence are not clearly grouped together for use in the first and second product-sum calculating means.”

It is respectfully submitted that claim 1 has been amended in the manner suggested by the Examiner on the top of page 3 of the Action. In addition, claims 5, 7, 13 and 15 have also been amended in the manner suggested by the Examiner regarding this issue.

Further, it is respectfully submitted that claims 2, 7, 10, 13 and 15 have each been amended in the manner suggest by the Examiner by amending the claim language “said predetermined number of logic circuits” to – said logic circuits--. Moreover, while the Examiner has failed to address such, similar claim amendments have been made to claims 3, 5, 6, 8, 11, 14 and 16.

Further, with regard to claims 3, 6, 8, 11, 14 and 16, such claims have been amended to clarify that the load capacitance of one logic circuit is smaller than the load capacitance of the one respective storage circuit. In addition, the Examiner takes the position that “the measure of load capacitance may be interpreted to be an input or an output load capacitance and should be amended to be more definite.”<sup>1</sup> It is respectfully submitted that lines 17-20 of page 27 of the present specification call for “[i]f the logic gate circuit has its load capacitance smaller than that of the storage register, the logic gate circuit consumes less power than the received signal storage register when the unnecessary signals are input, providing reduction of power consumption as a whole.” (Emphasis added.) In view of such, claims 3, 6, 8, 11, 14 and 16 have been further amended to specify that the load capacitance is input load capacitance to overcome this portion of the Examiner’s objection.

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<sup>1</sup> Please see, lines 18-20, page 3 of the Action

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Therefore, it is submitted that the amendments to claims 1-3, 5-8, 10, 11 and 13-16 overcome all the claim objections to claims 1-3, 5-8, 10, 11 and 13-16 set forth in item 4, pages 2-5, of the Action. Accordingly, withdrawal of these claim objections is respectfully requested.

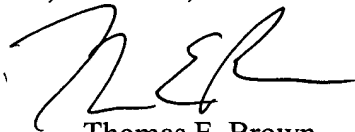
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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